REMARKS

Applicants have amended claims 1 and 13. No claims were added or cancelled. Accordingly, claims 1-19 remain pending in the present application. Applicants have amended the title of the invention as suggested by the Office Action.

Rejections under 35 USC 102(e)

The Office Action rejects Claims 1-19 under 35 USC 102(e) as being clearly anticipated by Duluk Jr. et al. '730 ("Duluk").

The streaming memory system presented in Applicant's invention reorders memory references in a very particular way. Applicants invention selects the next memory operation to be presented to the memory system from a set of pending memory operations. In other words, the memory order is determined as memory references *leave* the memory controller. Claim 1, as amended, highlights this feature of the invention, namely, in reciting "a control circuit that selects a memory reference from a set of pending memory references in said address buffer." Duluk on the other hand determines memory order as references arrive at the memory controller and does this using a separate conflict detector mechanism.

Duluk does not disclose a control circuit such as the one recited in now amended claim 1. Duluk sorts incoming memory references into two groups as they arrive: conflicting and non-conflicting. All of the non-conflicting references are first performed in-order, then all of the conflicting references are performed in-order.

Specifically, referring to Figure 13(b) of Duluk, which is cited by the Office Action as disclosing Applicant's control circuit of claim 1, the memory references are examined in order as they arrive and classified as conflicting or non-conflicting by the conflict detector (2602) at that time. If the memory reference is non-conflicting, then it is stored in the reorder queue (2603) and the RdXQ (2606). Memory accesses are presented to the RMC (2649) in order from the RdXQ (2606). If the memory reference is conflicting, it is placed in the ConfQ (2604) and dealt with only after 32 accesses have been classified. After the non-conflicting accesses from the group of 32 accesses are all placed in the RdXQ (2606), the conflicting accesses are placed into the RdXQ (2606), in the order they were originally presented to the

memory system. This has the effect of performing some limited memory reordering in which non-conflicting accesses will be presented to the RMC (2649) in the order that they arrived, and conflicting accesses will also be presented to the RMC (2649) after all non-conflicting accesses, but still in the order that they arrived.

Applicant's memory system differs substantially from this by at each point in time selecting the next memory operation to be performed from among a set of memory references in the address buffer, as recited in amended claim 1. For these reasons cited above, Applicants respectfully submit that claim 1 is allowable over Duluk and request that the rejections under 35 USC 102(e) be withdrawn. Likewise, since claims 2-12 depend from claim 1, which Applicants have demonstrated to be allowable over the cited reference, these claims are also allowable.

Further, Applicants have amended claim 13 to more clearly point out this feature of the invention. Claim 13 now recites the step of "selecting a memory reference from among a set of pending memory references and presenting this memory reference to said memory array". This is nowhere disclosed in Duluk. For this reason and the reasons presented above with respect to claim 1, Applicants submit that claim 13 and claims 14-19, which depend from claim 13, are allowable. Therefore, Applicants request that the rejections under 35 USC 102(e) be withdrawn.

Applicants respectfully submit that all pending claims are in condition for allowance and request a notice to that effect.

Respectfully submitted,

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APPENDIX WITH MARKINGS SHOWING CHANGES MADE

IN THE TITLE

The title of the invention is changed as follows:

[STREAMING MEMORY SYSTEM] **SYSTEM AND METHOD FOR RE-ORDERING MEMORY REFERENCES IN A MEMORY CONTROL SYSTEM TO SPEED ACCESS TO MEMORY CELLS**

IN THE CLAIMS

The claims are amended as follows:

1. (Amended) A memory system that receives addresses corresponding to data in an order comprising:

an address buffer that receives addresses in said order;

a memory array;

a control circuit that selects a memory reference from a set of pending memory references in said address buffer to present to the memory array, said references being presented [presents addresses] to [the] said memory array in an order different than the order in which they were received [by the address buffer]; and

a read buffer, that receives data read out from the memory array.

13. (Amended) A method [Method] of accessing memory comprising the steps of:

receiving a sequential plurality of memory access requests in the form of an address inputs;

buffering the plurality of address inputs;

initiating an out of order memory access request to a memory array for one of the sequential plurality of memory access requests such that one of the plurality of address inputs is requested in an order different than the order in which the one address was received;

selecting a memory reference from among a set of pending memory references and presenting this memory reference to said memory array; and

buffering read results of those memory access requests corresponding to read operations.